GaAs ULTRA HIGH FREQUENCY DIVIDERS WITH ADVANCED SAINT FETS

K. Osafune, T. Enoki, K. Yamasaki and K. Ohwada

NTT Electrical Communications Laboratories
3-1, Morinosato Wakamiya, Atsugi-shi,
Kanagawa Pref., 243-01 Japan.

ABSTRACT

Circuit design, fabrication and performance of ultra high frequency dividers with GaAs BFL circuits are described. 10.6 GHz operation at 258 mW is achieved using a new self-aligned gate, GaAs FET process, called Advanced SAINT, which avoids excess gate metal overlap on the dielectric film and air-bridge technology, due to a reduction of gate and interconnection parasitic capacitance. Furthermore, the possibility of above 20 GHz high frequency operation for GaAs MESFET frequency dividers is predicted by circuit optimization and FET improvements including parasitic capacitance reduction and transconductance enhancement.

INTRODUCTION

High speed GaAs LSIs, such as the 16 kb SRAM(1) and 2 Gb/s time switch(2) have been developed with SAINT FETs(3). GaAs MSIs and SSIs have great potential in satellite and microwave communications systems because of their ultra-high frequency operation, low power consumption and radiation hardness. For the local oscillator circuits in such systems, a frequency divider operating at a higher frequency and with lower power is required to simplify the phase locked loop.

Various circuit configurations for GaAs ultra high frequency dividers, such as BFL(4), SCFL(5), and DCFL(6), have been previously investigated. BFL circuits have the advantages of high speed operation and simple configuration, consisting of only MESFETs, since diodes are constructed by the same MESFETs with connection between the source and drain. In addition, BFL circuits have high driving capability.

In this paper, circuit design, fabrication and performance improvements of a GaAs BFL ultra high frequency divider described. As a result of circuit optimization, a binary frequency divider using BFL circuits with a source follower proved to operate faster than one having only level shift diodes. Therefore, the former circuit configuration was adopted. For parasitic capacitance reduction, a new FET process, called Advanced SAINT(7), has been developed. It utilizes a self-aligned gate formation technology so as to avoid the excess gate metal overlap upon dielectric film which causes parasitic capacitance in conventional SAINT FETs(3). The second level interconnection lines have been constructed by air-bridge technology, minimizing parasitic capacitance between lines.

Using these technologies, BFL M/S binary frequency dividers were fabricated with 0.5 μm gate FETs and operated at 10.6 GHz with 258 mW power dissipation. In addition, the potential operation of GaAs MESFET static frequency dividers above 20 GHz is also described.

CIRCUIT DESIGN

Two types of BFL circuits consisting of different output circuit configurations, (A and B)(4) were studied. These circuit configurations are shown in Fig.1. Type A circuit uses a source follower in the level shift position to ensure a large driving capability. Type B circuit uses only diodes in the level shift position. These circuits were applied to a two-level series gating master-slave, flip-flop circuit considered to be capable of the highest frequency operation. High frequency operation of the binary frequency dividers with BFL circuits A and B were simulated under standard supply voltages of V_{DD} 3 V and V_{SS} -2 V by improved SPICE II, using FET and diode models including parasitic capacitance(8). Results indicating dependence of maximum operation frequency fc.max on driver FET gate width W_g are shown in Fig.1. It can be seen that the frequency divider constructed with type A BFL circuits, enabling large driving capability, allows approximately 1 GHz improvement in operation frequency compared to type B BFL circuits. As shown in Fig.2, type A BFL circuits for binary frequency dividers were used in our experiments, along with W_g 40μm, as the maximum operation frequency showed a saturation tendency at 30μm.

Figure 3 shows circuit simulation results of the dependence of the maximum operation frequency on FET gate parasitic capacitance, C_p, using standard supply voltages, with or without interconnection capacitance. In the conventional SAINT FET, C_p was estimated to be 16 fF/40 μm gate width as measured from the frequency divider. It is expected that the reduction of parasitic capacitance will be remarkably effective for high-frequency operation.

Maximum operation frequency dependence on FET transconductance was simulated with reduced

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FET and interconnection parasitic capacitance. As shown in Fig. 4, a maximum operation frequency higher than 20 GHz is predicted at a gate length of 0.2 μm and a transconductance of 400 mS/mm, attainable by gate length shortening and active layer thinning.

FABRICATION PROCESS

Schematic cross-sectional views of conventional and Advanced SAINT FETs are shown in Fig. 5. In the Advanced SAINT FET structure, there is no gate metal overlapping, the cause of parasitic capacitance in the conventional SAINT FET.

The Advanced SAINT fabrication process(7) is almost the same as the conventional(3) except for gate formation. The gate electrode formation process involves the following steps: (i) Mo and Au are deposited onto the whole surface by sputtering. (ii) The Au surface is planalized by ion beam milling with a large beam incident angle. (iii) Using this Au pattern as the etching mask, Mo film is selectively etched by RIE. Consequently, the gate electrode is embedded, in a self-aligned manner only in the gate contact region. After gate formation, source and drain ohmic electrodes were formed by AuGe/Ni deposition and sintering.

With self-aligned gate electrode formation, FETs having a gate-length of only 0.2 μm were successfully fabricated without excess gate metal overlap on the dielectric film. The decrease in gate parasitic capacitance C_p, estimated from frequency divider measurements, was 13 fF/40 μm gate-width. This reduction is thought to be due to the removal of excess gate metal overlaps by self-aligned gate electrode formation.

In addition to FET structural improvements, second level interconnection lines were constructed using "air-bridge" technology. Though two level interconnection technology using SiN or SiO_2 as the interlayer is popular, the high dielectric constant of the interlayer increases between line capacitance and degrades IC high frequency performance. In order to minimize between line capacitance, it is necessary to construct the second level interconnection line by "air-bridge" technology, which yields an ideal interlayer dielectric constant. An SEM photograph of the air-bridge lines is shown in Fig. 6.

Binary frequency dividers were fabricated with Advanced SAINT and air-bridge technology. The gate length and the threshold voltage of FETs respectively, were 0.5 μm and -1 V, where the transconductance was 200 mS/mm. Although the fabrication of an 0.2 μm gate-length FET could be achieved by using Advanced SAINT technology, the yield was insufficient for frequency divider ICs. To date, only the use of 0.5 μm gate-length FETs for IC fabrication has been achieved. Ultra high frequency divider ICs with 0.2 μm gate-length Advanced SAINT FETs are now under fabrication. The circuit geometry was optimized and made compact by symmetric circuit arrangement and short interconnections. A photograph of a fabricated circuit is shown in Fig. 7. Chip size is 1x1 mm^2.

MEASUREMENT RESULTS

High-frequency measurements were carried out with a high-frequency probe card at room temperature. Under standard biases of V_{DD} 3 V and V_{SS} -2 V, the maximum operation frequency was 9.6 GHz, as shown in Fig. 8(a), which corresponds to the simulation results (Fig. 4). Under optimized supply voltages of V_{DD} = 3.4 V at 48 mA and V_{SS} = -3.1 V at 30 mA, a maximum toggle frequency of 10.6 GHz was obtained at 258 mW power dissipation, as shown in Fig. 8(b)(9). The internal logic swing was 180 mV_{p-p} in the dividing operation shown in Fig. 8(b), though the output swing was as small as 24 mV_{p-p} because a 50 ohm load was used at the point of measurement. A lower power dissipation will occur in the case of a threshold voltage higher than -1 V. The maximum toggle frequency is 4 GHz higher than that of a frequency divider, 6.8 GHz, the latter consisting of identically-sized FETs fabricated by conventional SAINT and conventional two level interconnection technology with a SiN interlayer dielectric film(10).

CONCLUSIONS

Aiming at ultra-high frequency operation, a frequency divider circuit design, the reduction of FET and interconnection parasitic capacitance were studied. Advanced SAINT, having gate electrodes without excess overlap upon dielectric film, and applied air-bridge technology successfully reduced parasitic capacitance around the gate and between interconnection lines. Using these technologies, at room temperature, a BFL binary frequency divider with 0.5 μm gate FETs achieved 10.6 GHz operation at 258 mW.

Circuit simulation with empirical FET parameters predicts the possibility of high frequency operation above 20 GHz for GaAs static frequency dividers using Advanced SAINT FETs with an 0.2 μm gate length and air-bridge interconnections. This divider IC using GaAs BFL circuits can be effectively applied to satellite and microwave communications.

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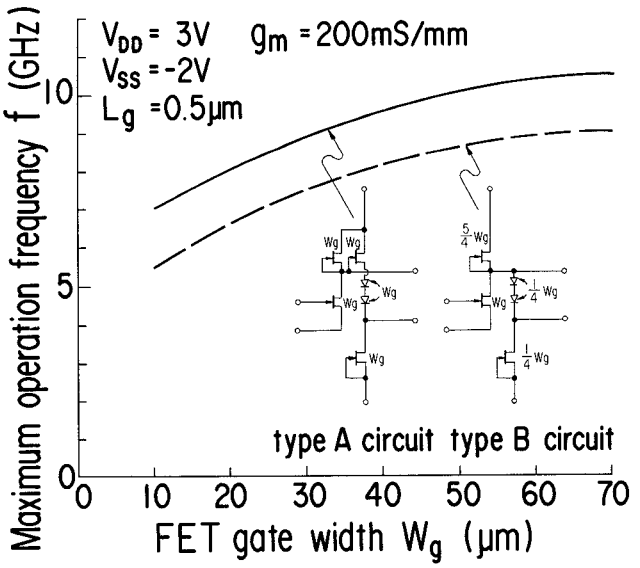


Fig. 1 Maximum operation frequency dependence of two types of frequency dividers on driver FET gate width. Type A BFL circuit uses a source follower in the level shift position to ensure a large driving capability. Type B BFL circuit uses only diodes in the level shift position.

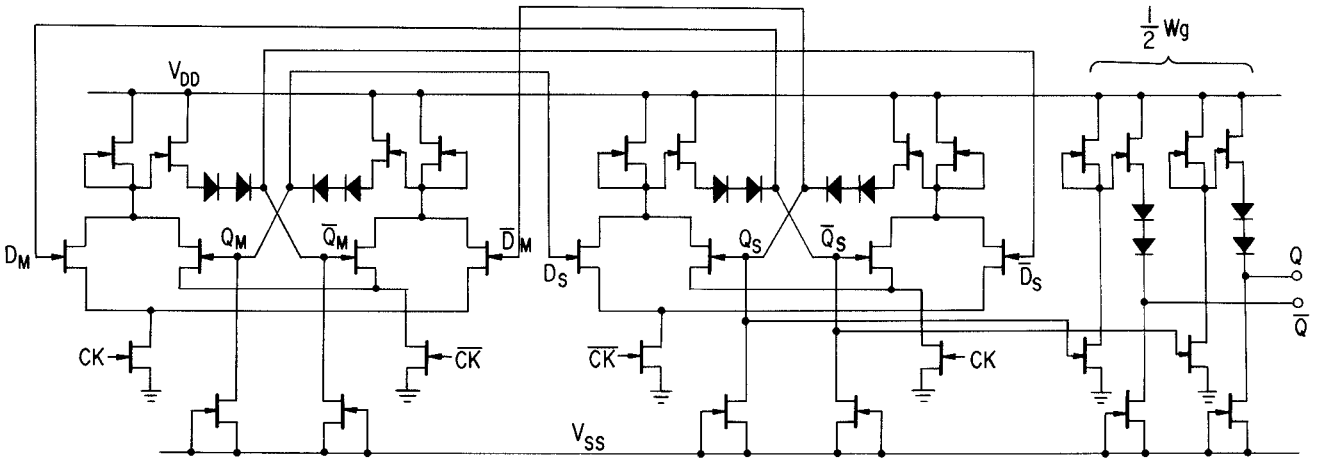


Fig. 2 Schematic diagram of a binary frequency divider with output buffers.

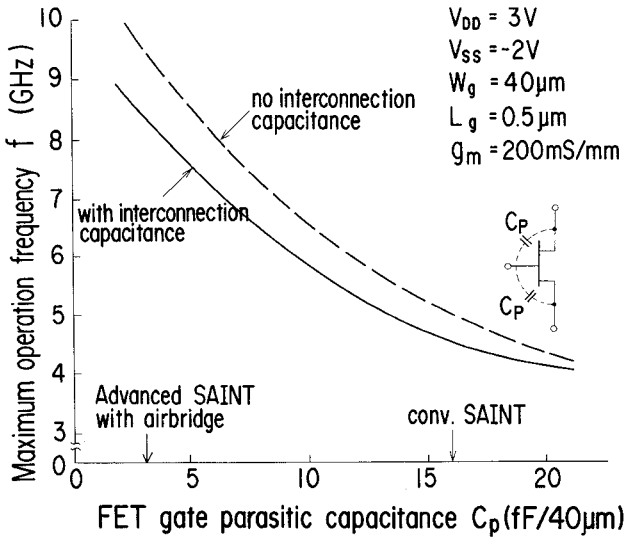


Fig. 3 Simulated maximum operation frequency dependence on FET gate parasitic capacitance with or without interconnection capacitance.

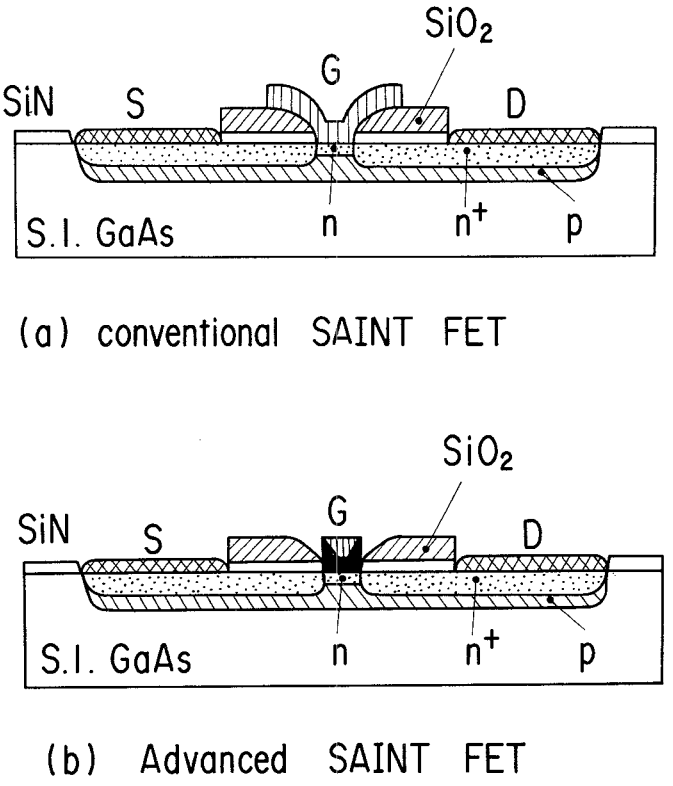


Fig. 5 Cross sectional views of (a) a conventional FET and (b) an Advanced SAINT FET.

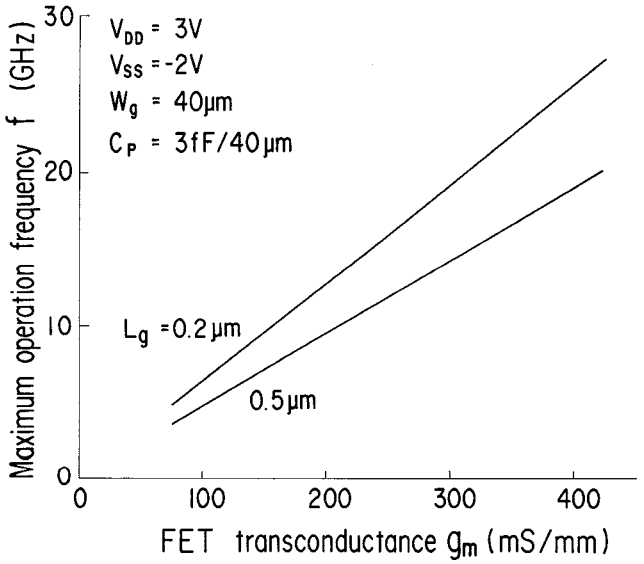


Fig. 4 Simulated maximum operation frequency dependence on FET transconductance with reduced parasitic capacitance.

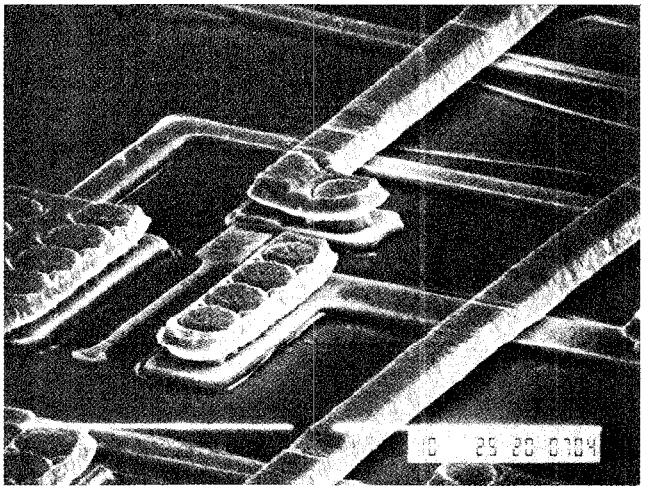


Fig. 6 SEM photograph of air-bridge lines.

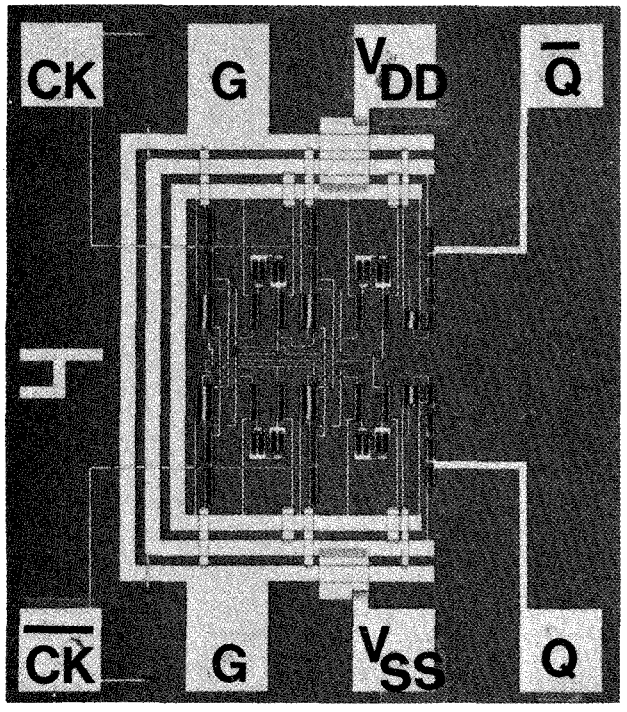
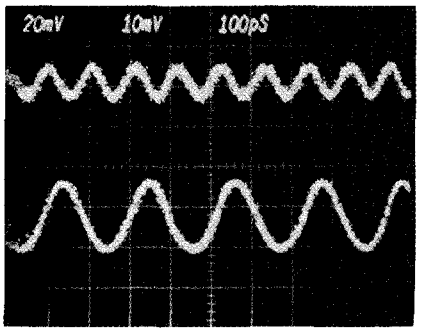
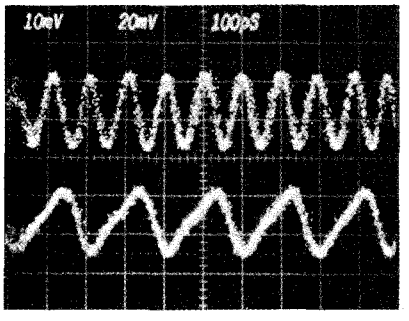


Fig. 7 Microphotograph of BFL M/S binary frequency divider. Chip size is 1x1 mm^2.



(a)V_{DD} 3 V, V_{SS} -2 V,
Power dissipation : 200 mW,
Clock input : 9.6 GHz, 1.2 V(peak-peak),
Output : 180 mV(peak-peak).



(b)V_{DD} 3.4 V, V_{SS} -3.1 V,
Power dissipation : 258 mW,
Clock input : 10.6 GHz, 1.1 V(peak-peak),
Output : 24 mV(peak-peak).

Fig. 8 Operation wave forms of a BFL M/S binary frequency divider.